**Week 4(TTL)**

## **Question No. 1**

## 

**For the given TTL NAND circuit, assume common emitter current gain, *βF* = 25 and reverse common emitter current gain of the transistors *βR* = 0.1 . Assume *VOH* =3.4 *V* and *VOL*=0.1*V* and for saturation mode, *VBE*=0.8*V*, *VCE*=0.1*V.***

|  |  |
| --- | --- |
| (a) | Assume no Loads are connected to the driver device. If at least one input is low (0.1*V*), find ***i1 , iB2 , i2 , iBo* and *i3  in mA.*** |
| (b) | Repeat the calculation of (a) if both the inputs are high (*vX* = *vY* =5 *V*) |
| (c) | Find the maximum possible fanout of this TTL circuit. |
| (d) | Assume all inputs of the **Driver** circuit are high.  (i) Find the maximum fanout if the “other” input of the **load, VY = 5V (High)**.  (ii) If **both inputs** of the **Load** circuits = **0.1 V**, then what would be the maximum fanout?  Compare and comment on the above two cases to identify which case has better fanout and why? |
| (e) | Find the power dissipation in Driver for all cases [Assume 4 loads are connected to driver’s output] |

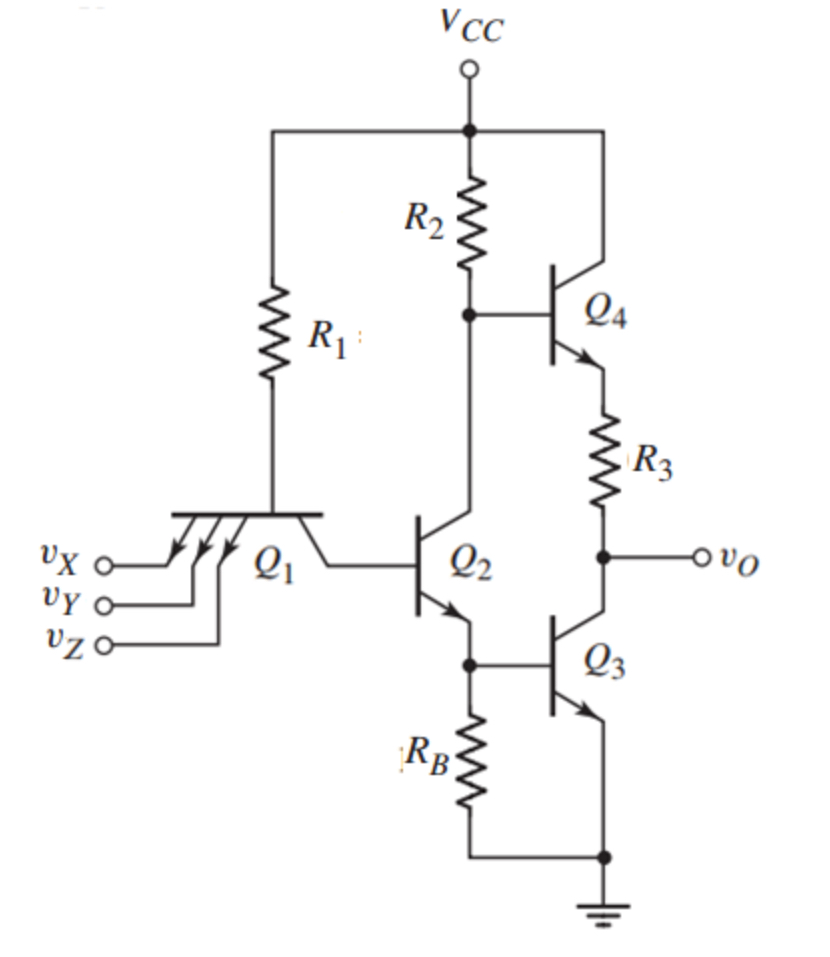
## **Question No. 2**

## 

**For the given TTL circuit with totem-pole output, assume common emitter current gain, *βF* = 25 and reverse common emitter current gain of the transistors *βR* = 0.1 .**

|  |  |
| --- | --- |
| (a) | Find the value of  ***βMin*** for transistor Q2  so that Q2 can remain in saturation when both input is HIGH. |
| (b) | Assume inputs of the load devices are not connected to driver device. If at least one input is low (0.1*V*), find ***i1 , iB2 , i2 , iBo* and *i3  in mA.*** |
| (c) | Repeat the calculation of (b) if both the inputs are high (*vX* = *vY* =3.6 *V*) |
| (d) | Find the maximum fanout of this TTL circuit for the case mentioned in (c) |
| (e) | Find out the maximum power dissipation of the TTL circuit in *mW* when no load is connected. |
| (f) | Calculate maximum fanout for Vx = VY = 0.1V. Given that VOH (No load) =3.6V. And, from this calculation prove that T4 is in **forward active mode**. |

## **Question No. 3**



**For the given TTL circuit, given *R*1 = 3.0 *k*Ω, *R*2 = 1.3 *k*Ω, *R*3 = 0.55 *k*Ω and *RB* = 8 *k*Ω. assume, VCC = 3.5 V, common emitter current gain, *βF* = 15 and reverse common emitter current gain of the transistors *βR* = 0.8 .**

|  |  |
| --- | --- |
| (a) | If all inputs are High (*vX* = *vY* =*vZ* = 3.5 *V*), find ***iB1 , iB2 , iB3 , iB4* and *iE3  in mA.*** |
| (b) | Assume inputs of the load devices are not connected to the driver device. If at least one input is low (0.1*V*), find ***i1 , iB2 , i2 , iBo* and *i3  in mA.*** |
| (c) | Find out the power dissipation of the TTL circuit in *mW* for both (a) and (b). |
| (d) | Find the maximum fanout of this TTL circuit for the case described in (a). |
| (e) | If at least one input is low (0.1*V*) and **12 loads** are connected to the output, find the new value for ***vo***. |

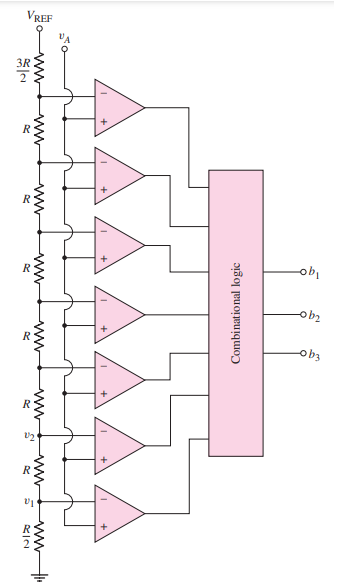
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# **Week 5(ADC and DAC)**

## **Question No. 1**

|  |  |
| --- | --- |
| (a) | An analog signal in the range −1V to 16V is to be converted to a digital signal with a quantization error of less than or equal to 0.781% of the input voltage range for quantization. **e.g the overall quantization error for this input signal should be less than or equal to 0.781% of the ADC’s maximum quantization error.** The quantization error is the maximum error occurring after quantizing the analog signal.  **Find** the required number of bits for the above expression. |
| (b) | **Determine** the minimum sampling frequency of a signal. |

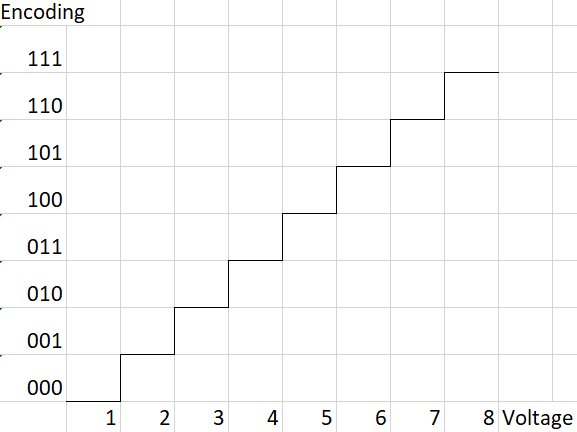
## **Question No. 2**

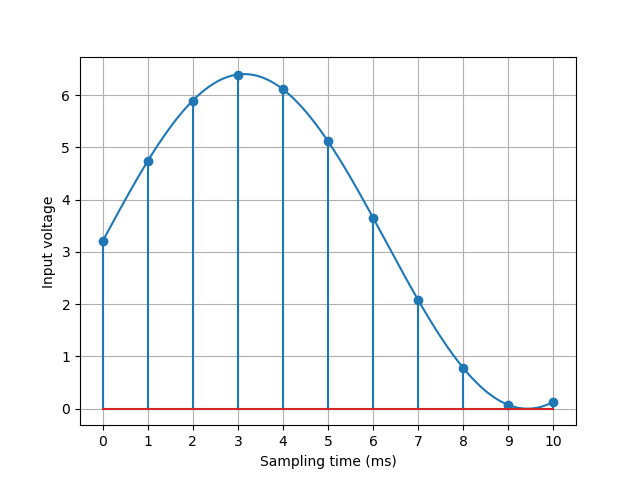


Design a 3 bit flash ADC with a reference voltage of *VREF*=10*V*. The quantized levels for this ADC should be **uniform (Equal step size).**

|  |  |
| --- | --- |
| (a) | **Calculate** total number of resistors and comparators required to fabricate a 3-bit flash A/ D converter. |
| (b) | Calculate the 1LSB value or each step size (quantization range) for this 3 bit ADC. What would be the resolution for this ADC? |
| (c) | Calculate each **quantization level** and plot the **Vin vs Dout** graph. |
| (d) | If the input voltage **Vin= 7 V,**  i) Comment on the **quantization range** in which the input lies.  ii) Find the **digital output** for the given input. |
| (e) | If the 3-bit output is 110.What is the maximum and minimum value of *vA* that produces this output?(Hint:find the quantization range). |
| (f) | If 1 bit was increased from this 3 bit Flash ADC, how many resistors and comparators are required? comment on the hardware changes for this 1 bit of increment. |

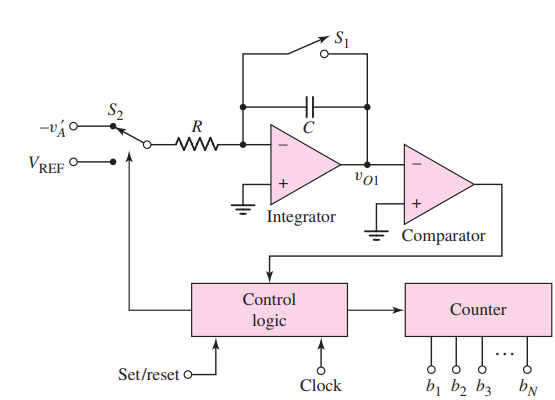
## **Question No. 3**





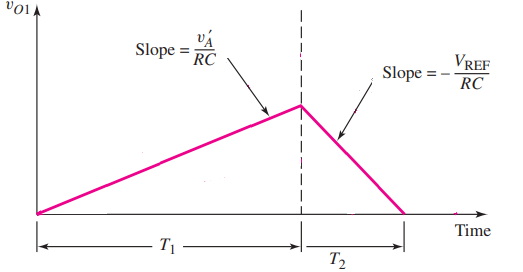
|  |  |
| --- | --- |
| (a) | Design a 3-bit Flash ADC circuit for the given input-output characteristics. |
| (b) | An unknown signal is passed to the ADC as input. The ADC takes samples at a rate of 1kHz. In the graph, the input signal is shown where the x-axis represents time, and the y-axis represents the voltage at any specific time. The sampling instances are given in the figure. Find the encoded output that represents the analog signal inside the given time frame. |

## **Question No. 4**



A 8 bit dual slope ADC has Vref = 5V, and an 8 bit counter that outputs an 8-bit representation of the input signal. A 1MHz clock is used for the control and counter circuits.

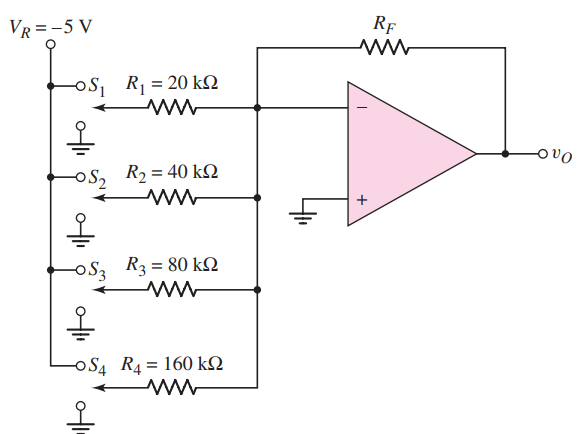
|  |  |
| --- | --- |
| (a) | Determine the input voltage range, number of steps and step size (resolution)of the ADC. |
| (b) | For a specific input, the ADC outputs a count of m=100. Determine the input voltage. |
| (c) | Determine the total time required to get the reading in (b). [Hint: it is how much time it would take to produce the output from the moment switch S2 is connected to (−v′A)] |
| (d) | Calculate the maximum sampling frequency of the ADC. |
| (e) | A person wishes to get a sampling frequency 4 times that of the current circuit. Determine how many bits should be used for the counter without changing any other system parameters. |
| (f) | What is the digital output if the input ( *v*′*A*) =3.0000*V*? |



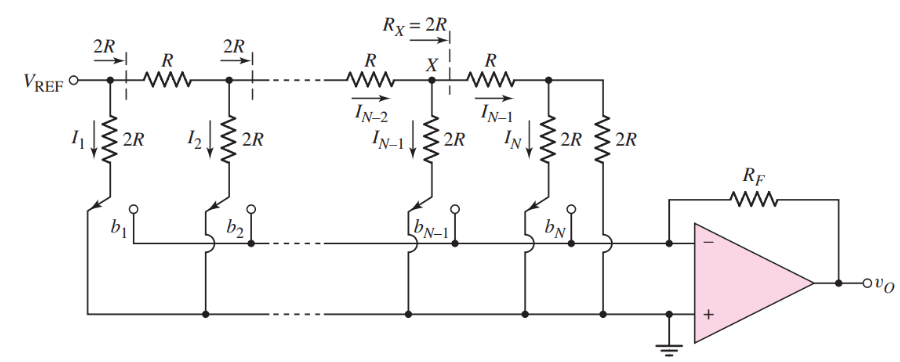
|  |  |
| --- | --- |
| (a) | Find the value of *vO*1 at *t*=*T*1, suppose *R*=25*k*Ω and *C*=2*μF*. |
| (b) | If R= 50 *k*Ω and we *C*=2*μF,* calculate the new value of V01 at t=T1, compare it with (a) and comment on the changes between two output voltages. |

## **Question No. 5**

|  |  |
| --- | --- |
| (a) | **Determine** the output voltage, ***vo*** in V of the 4-bit weighted-resistor D/A in the following figure for input =1010 and input=1100? Assume RF= 5kΩ. |
| (b) | **Identify** the maximum allowed tolerance (± percent) in the value of  R1 so that the maximum error in the output is limited to **±LSB** quantized voltage value? (hint: Do two separate calculations for output error being **+LSB** and **-LSB** Then, calculate the percentage change in R1 in these two cases.) |



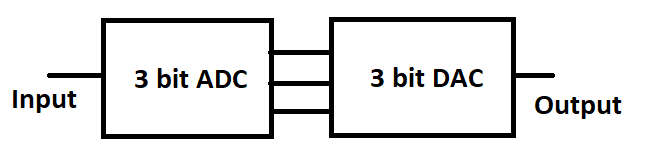
## **Question No. 6**



The *N*-bit D/A converter with an *R*–2*R* ladder network in the above figure is to be designed as a 6-bit D/A device. Suppose *VREF* =−5*V* and RF= R=5kΩ.

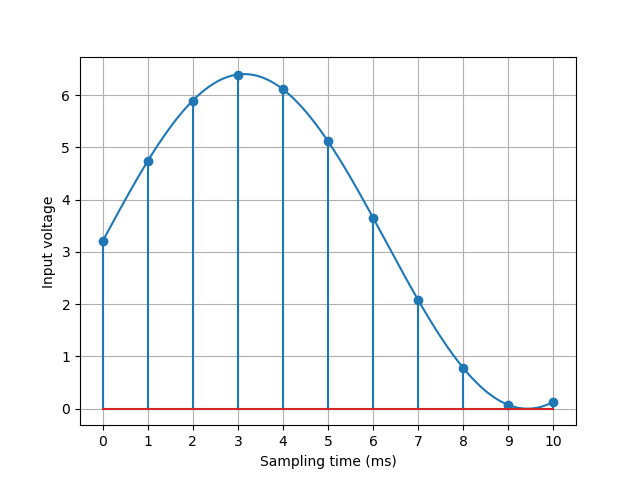
|  |  |
| --- | --- |
| (a) | Find currents ***I1,I2,I3,I4,I5*** and ***I6 .*** |
| (b) | What is the output voltage if the input is 010011? |
| (c) | What is the change in output voltage if the input changes from 101010 to 010101? |

## **Question No. 7**



|  |  |  |
| --- | --- | --- |
| ADC Input Voltage | Encoding | DAC Output Voltage |
| 0-1 | 000 | 0.5 |
| 1-2 | 001 | 1.5 |
| 2-3 | 010 | 2.5 |
| 3-4 | 011 | 3.5 |
| 4-5 | 100 | 4.5 |
| 5-6 | 101 | 5.5 |
| 6-7 | 110 | 6.5 |
| 7-8 | 111 | 7.5 |

|  |  |
| --- | --- |
| (a) | For the following input waveshape, draw the reconstructed output by the DAC. The sampling instances are marked on the input waveshape. |
| (b) | Comment on the quality of the reconstructed signal and how the quality would be affected if additional bits were used for both the ADC and DAC. |



## **Question No. 8**

Suppose we are using the DAC for audio output in a soundbox/speaker. We are allowed to replace **a single resistor** with a potentiometer/variable resistor to allow for volume control. Which resistor should be replaced for this?

## **Question No. 9**

Suppose a DAC circuit will have output voltage in the range of 0V-5V. Maximum allowable step size = 0.1V

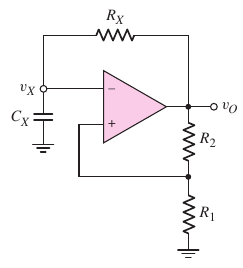
1. Assuming that the input voltages to the DAC can be 0V(low) or 5V(high), design a Binary weighted DAC circuit, number of input bits to be used and find the value of the resistors to be used.
2. Assume that an R-2R ladder circuit is to be constructed with only 10k and 20k resistor values. Find Vref and number of bits to be used for the design specifications.

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# Week 6( signal generator)

## 

## Question 1



The Dual Slope ADC in week 5 problem 4 uses a clock signal of **1 MHz**. Suppose, we want to supply this clock signal from a square-wave generator circuit. The square-wave generator circuit we studied in week 6 is a schmitt-trigger oscillator, as shown in the above figure.

Assume, the saturation output voltages of the om-amp are symmetric (i.e. equal in magnitude). Now, follow the steps stated below to design the circuit.

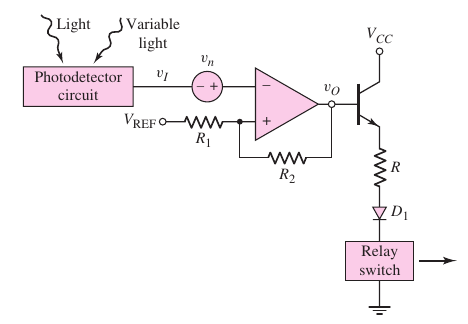
|  |  |
| --- | --- |
| (a) | Calculate the duty cycle of the circuit, considering symmetric output voltages. |
| (b) | Derive the expression of **Time Period, T** in terms of the circuit parameters. |
| (c) | Choose standard resistor and capacitor values to obtain the desired time period (or frequency.) |
| (d) | Calculate the deviation (in percentage) in frequency for your designed circuit. |
| (e) | How can we design a schmitt trigger oscillator circuit with a specific duty cycle (like 30%)? |

## Question 2

Previously, we designed a street light control circuit using a simple op-amp comparator. But it damaged some of the street lights.

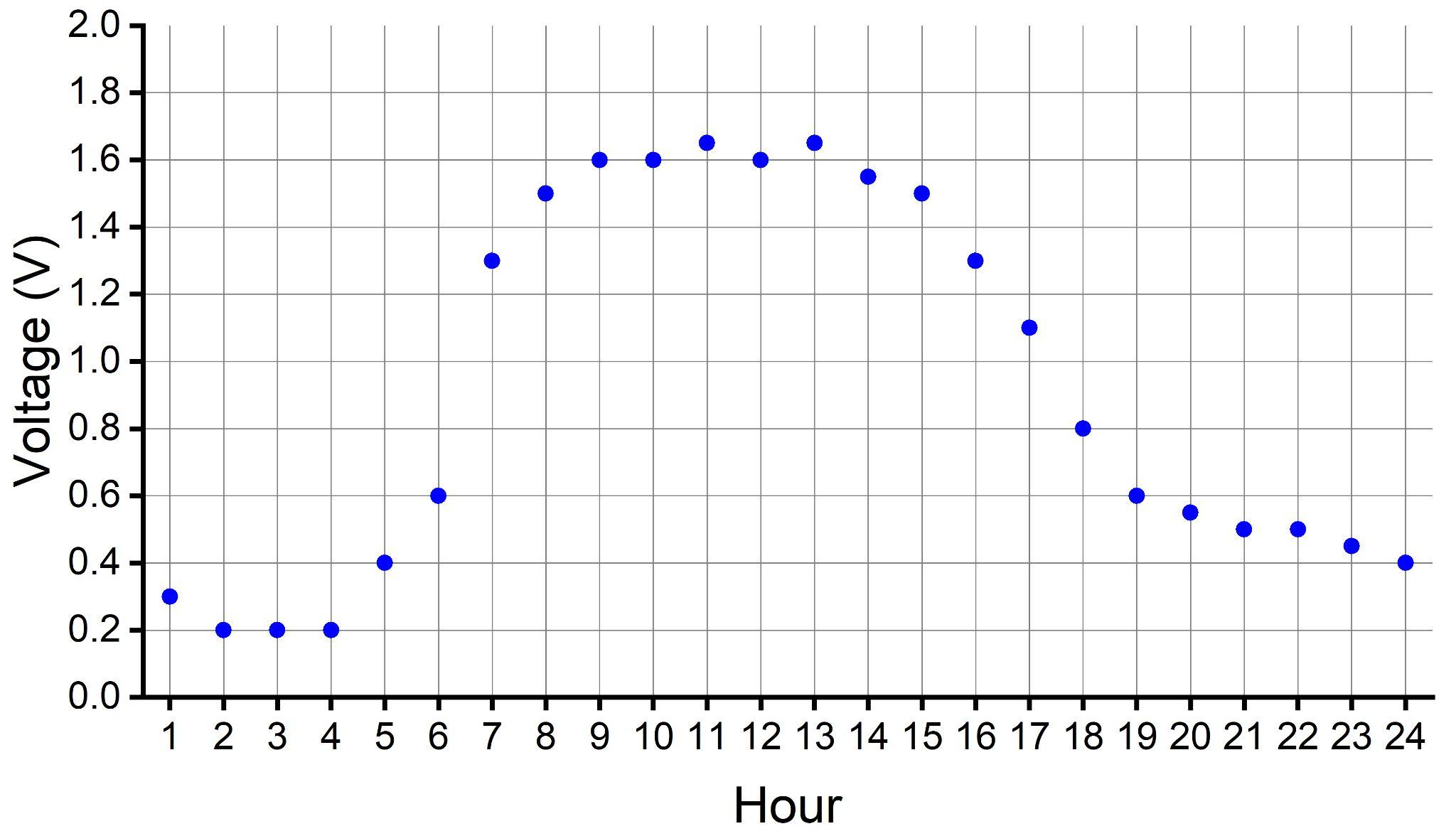
Now, we want to design a street light control circuit using Schmitt trigger, as shown below. This design employing Schmitt trigger circuit is robust to environmental noise and photodetector’s shot-noise, so hopefully it will not damage the street lights this time.

We want to install our street light control system in Mohammadpur, Dhaka. So, we went there last week to collect photodetector circuit data. Our collected data over 24 hours is shown in the plot below. Note that, the output voltage of a photodetector circuit is directly proportional to the amount of light incident on it and we use this output voltage as an input voltage of the schmitt trigger circuit.



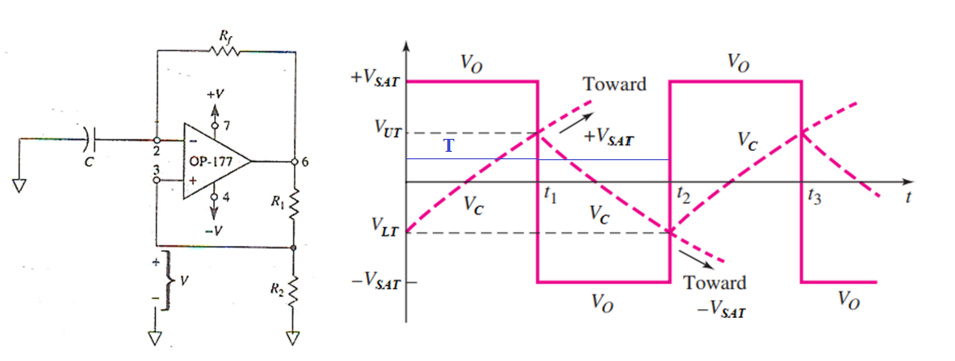
Now, help us in selecting the appropriate values of the circuit parameters.

|  |  |
| --- | --- |
| (a) | Choose an appropriate value of the switching voltage **VS .** |
| (b) | We found that the combined noise voltage has a peak-to-peak voltage of around 0.1 V. Considering this, choose an appropriate value of the hysteresis width of the schmitt trigger circuit. |
| (c) | For your chosen switching voltage and hysteresis width, select the values of **R1 , R2 , VREF**. |



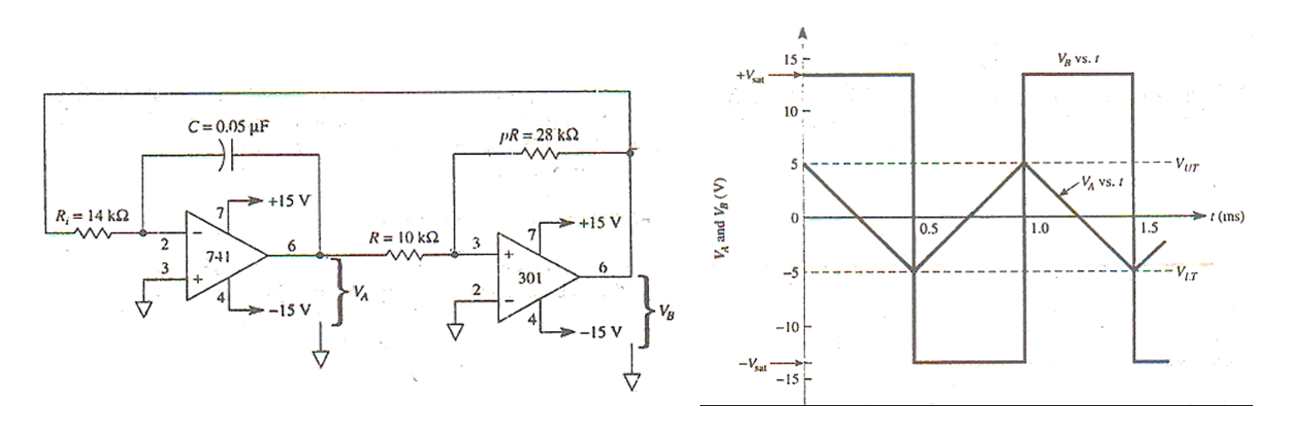
## **Question 3 :**

Assume for the square wave generator below, R2 = 0.86 \* R1 and +Vsat = -Vsat . Prove that T = 2RfC

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## Question 4 :

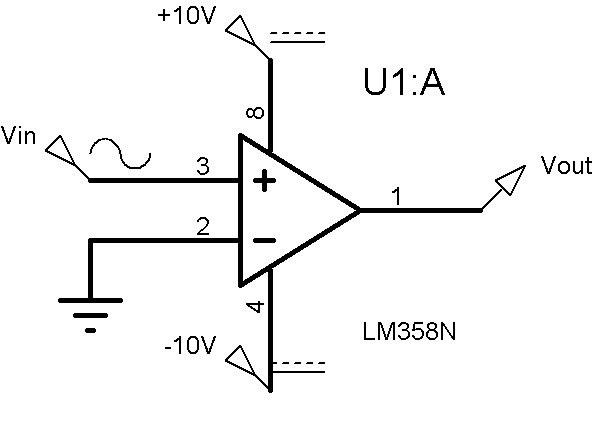
Assume for the triangular wave generator below, +Vsat = -Vsat . Prove that

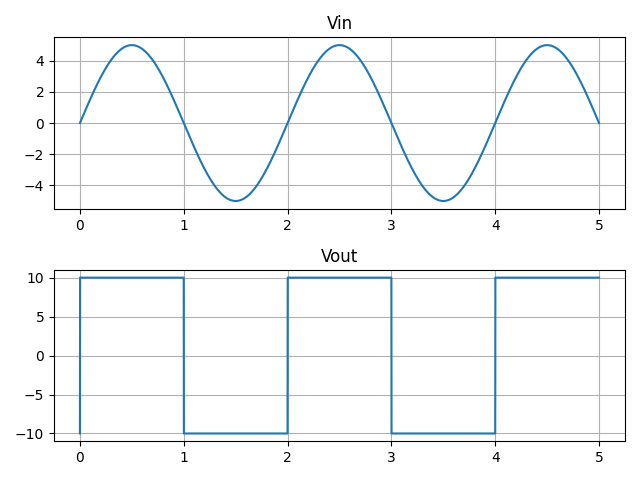


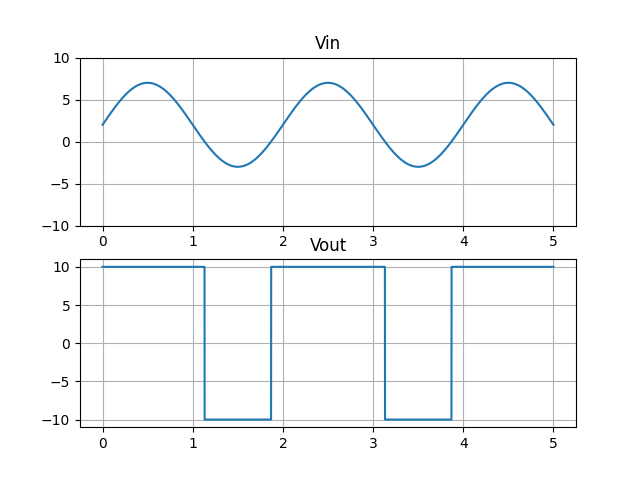
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## Question 5 :

For the OP-AMP comparator circuit below, Vin vs time plot is given. Draw the Vout vs time plot for the given input.

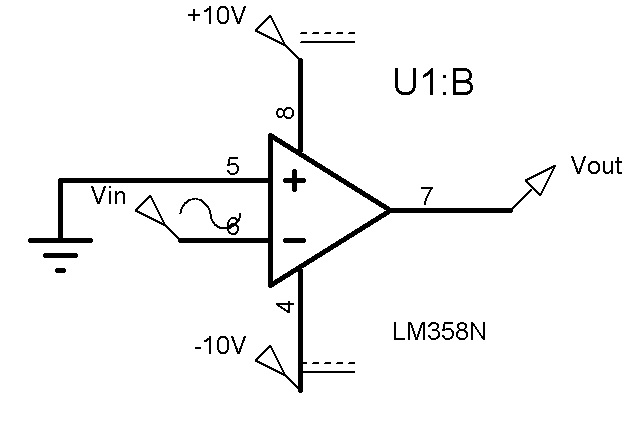


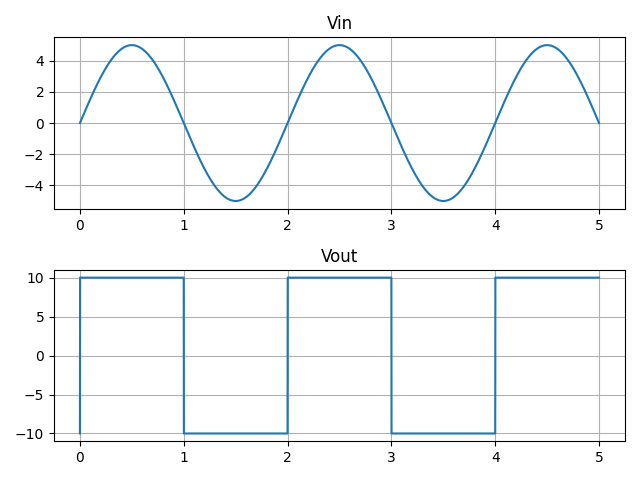
**(a)**

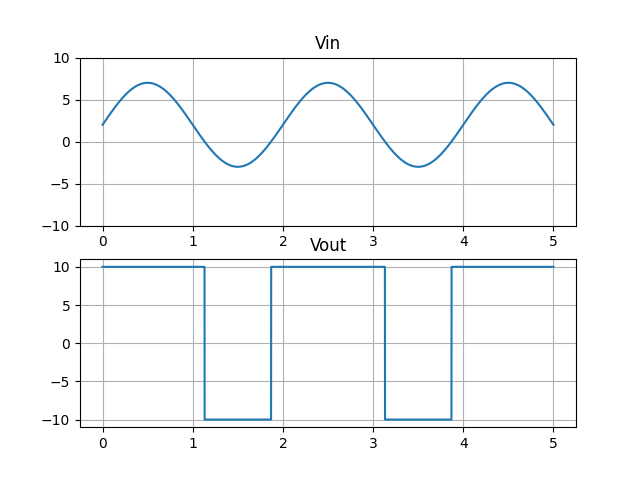
**(b)**

## Question 6 :

For the OP-AMP comparator circuit below, Vin vs time plot is given. Draw the Vout vs time plot for the given input.

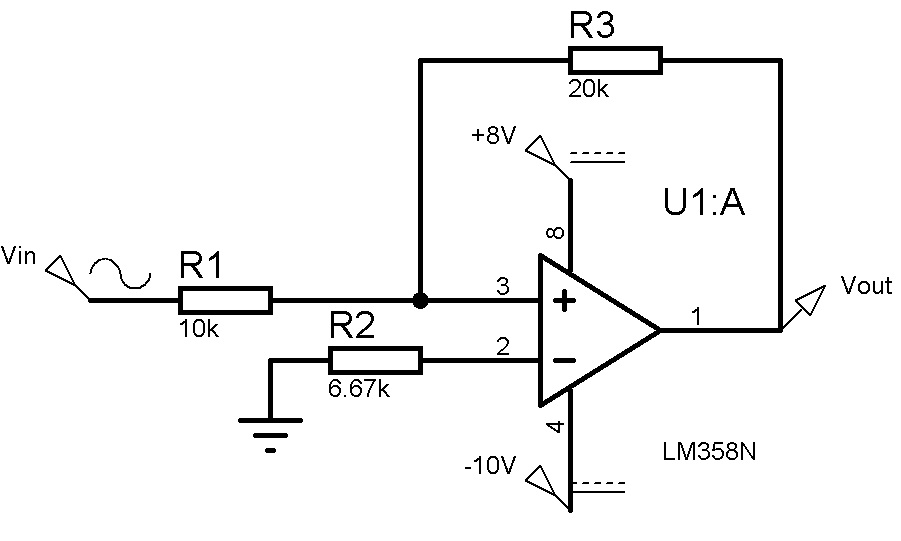


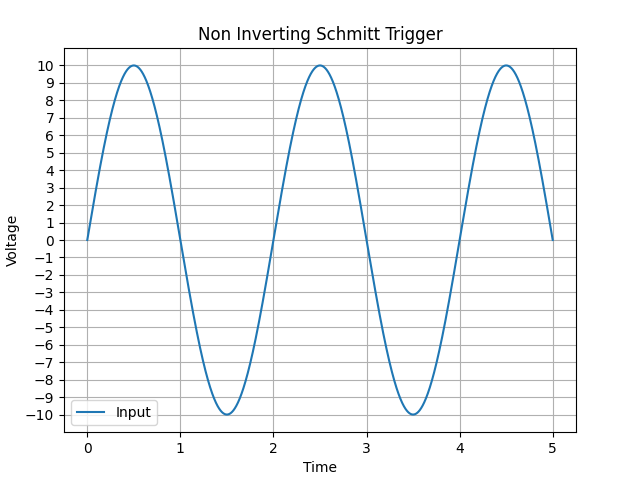
**(a)**

**(b)**

## Question 7 :

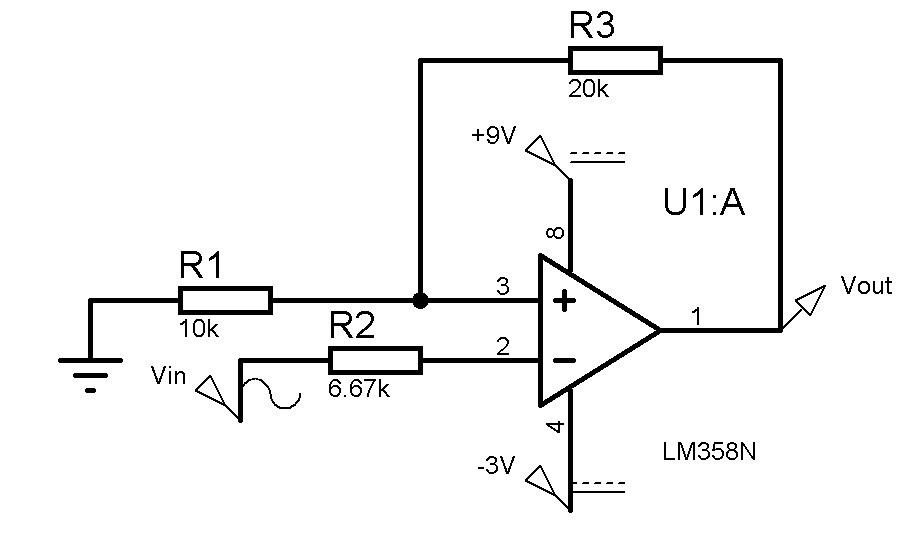
For the non-inverting schmitt trigger circuit below, Vin vs time plot is given. Draw the Vout vs time plot for the given input.

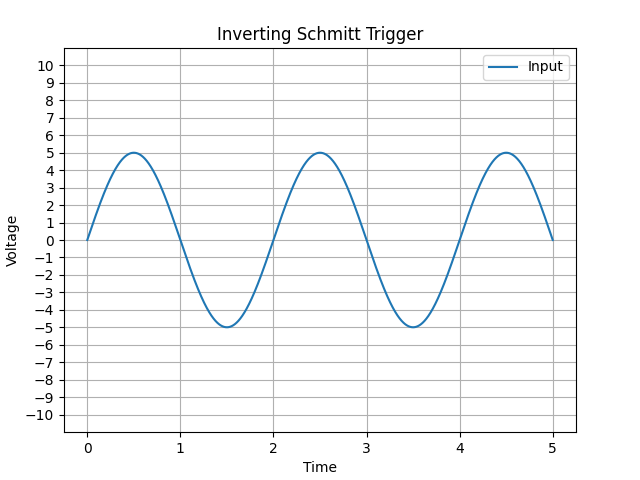




## Question 8 :

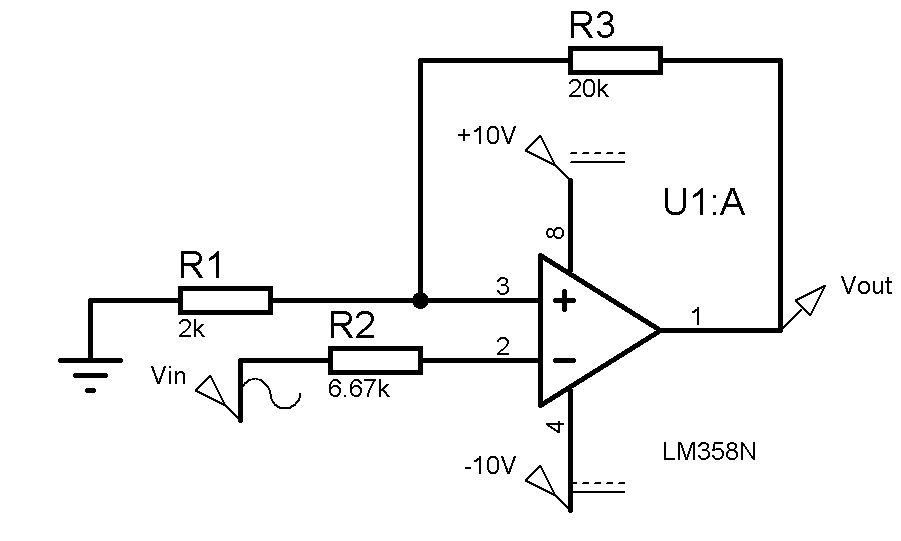
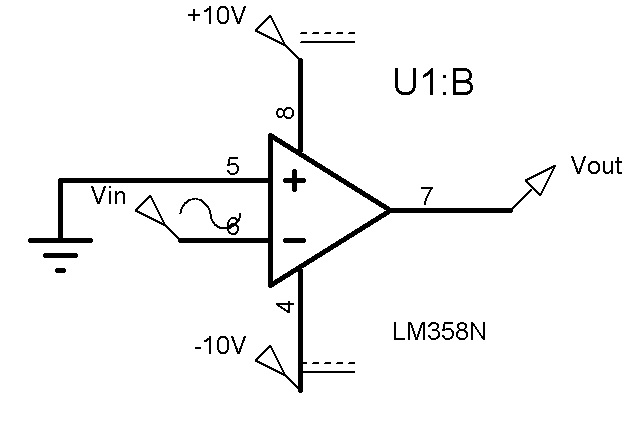
For the inverting schmitt trigger circuit below, Vin vs time plot is given. Draw the Vout vs time plot for the given input.

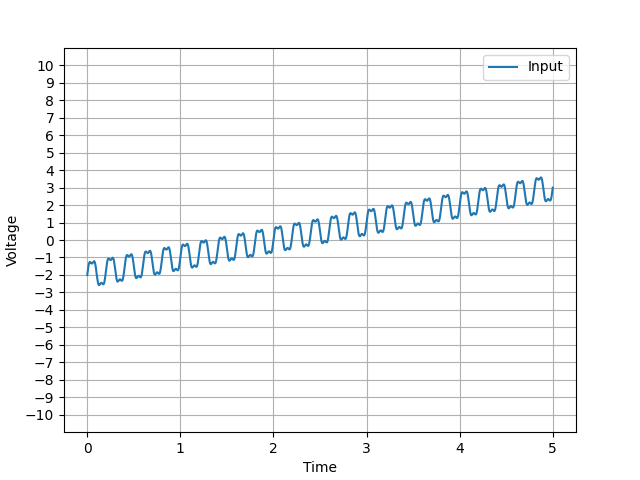




## Question 9 :

A light detector circuit has a sensor unit that generates a voltage proportional to the light intensity. You have been tasked with designing a circuit that will output high when the light level is low, and when the light intensity exceeds a certain threshold, the output will go low (turning off any artificial light). Two possible candidate circuits are 1. **Inverting Comparator** 2. **Inverting Schmitt Trigger** as given below. The signal from the light sensor is corrupted by interference from the AC power line as shown in the graph below.





|  |  |
| --- | --- |
| (a) | Draw the output if the inverting comparator is used for light intensity detection. |
| (b) | Draw the output if the inverting Schmitt trigger circuit is used. What is the interference voltage level that the Schmitt trigger can tolerate? |
| (c) | Which circuit is more appropriate for the use case and why? Explain from your results in (a) and (b) |

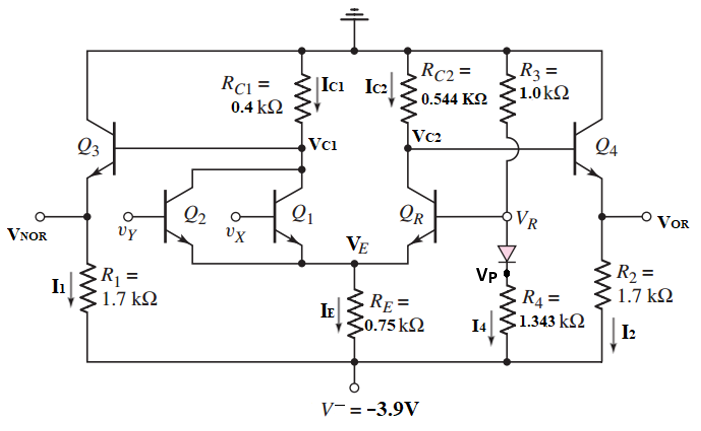
# Week 7 (ECL):

## Question 1:

For the ECL logic circuit above, ignore the base currents and assume Reference voltage, VR to be the average of logic high and logic low values. Also, assume when Q1 and Q2 are conducting, the B–C voltages of Q1 and Q2 are **-0.1V**.

|  |  |
| --- | --- |
| (a) | **Determine** the logical low and high voltages for the circuit. Also, calculate the possible value of reference voltage, VR. |
| (b) | **Determine** RC1 and RC2. |
| (c) | **Calculate** the power dissipated in the circuit for the following cases: (i) vx = vy = logic 1, and  (ii) vx = vy = logic 0. |

## Question 2:



For the ECL OR/NOR circuit above, ignore the base currents and assume Reference voltage, **VR** to be the **average** of logic high and logic low values.

|  |  |
| --- | --- |
| (a) | **Determine** the logic 0 and logic 1 voltage values for outputs VOR and VNOR. |
| (b) | When inputs VY and Vx are at Logical High, **calculate VP**, **I1**, **I2** and **I4**. |
| (c) | **Calculate** the power dissipated in the circuit for the case mentioned in (b). |

## Question 3:

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Consider the ECL circuit in above figure. Ignore the base currents.

|  |  |
| --- | --- |
| (a) | Determine RC2 such that v2 = −1 V when Q2 is on and Q1 is off. |
| (b) | For vin = −0.7, determine RC1 such that v1 = −1 V. |
| (c) | Find vO1 and vO2 for (i) vin = −0.7 V and (ii) vin = −1.7 V. |
| (d) | Find the power dissipated in the circuit for both the cases mentioned in (c). |

## Question 4:

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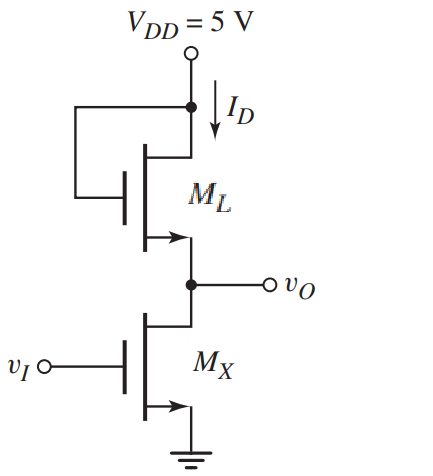
Consider the ECL circuit in the figure above, the logical high and low values are -0.7V and -1.4V respectively. Assume that the reference voltage VR is the average of the logical high and low values. Assuming transistor base currents are negligible, design the reference voltage generation circuit so that the currents through R5 and R2 are the same, and the reference voltage circuit power consumption is limited to 1mW. (Find the values of R1, R2 and R5)

# Week 8 (MOSFET):

## Question 1:

For the circuit below (enhancement Load Inverter), assume these parameters,

MOSFET process parameter for ML is **K’L= 5 μA/V2**, **(W/L)L = 2** and threshold voltage, **VTNL = 0.7V**. MOSFET process parameter for MX is **K’D= 25 μA/V2**, **(W/L)D = 4** and threshold voltage, **VTND = 0.7V**.



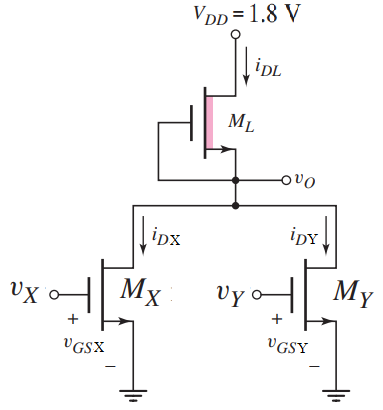
|  |  |
| --- | --- |
| (a) | Assume **VI = 5 V**. Find value of **Vo** in volt. Find **ID** and Power Dissipation. Verify the operating mode of **ML** and **MX**. |
| (b) | Now, assume **VI = 0.3 V**. Find **Vo**, **ID** , Power Dissipation and operating mode of **MX**. |
| (c) | What should be the value of **VI**  if we want **ML** to operate in the triode region? |

## Question 2:

For the circuit below (Depletion Load NOR), assume these parameters,

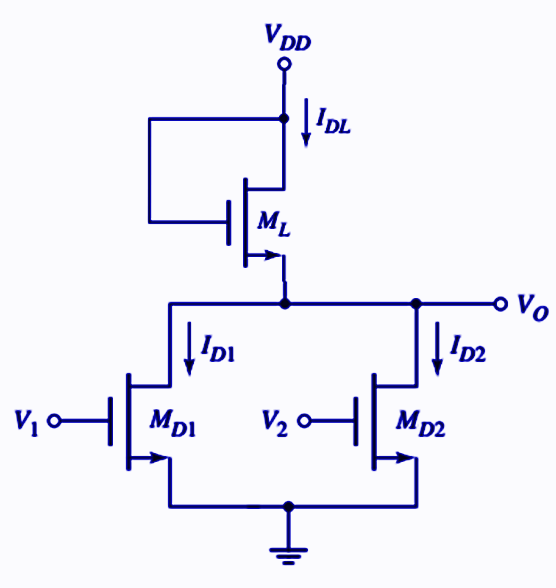
MOSFET process parameter for ML is **K’L= 50 μA/V2**, **(W/L)L = 2** and threshold voltage, **VTNL = −0.6V**. MOSFET process parameter for both MX and MY is **K’D= 33.25 μA/V2**, **(W/L)D = 4** and threshold voltage, **VTND = 0.4V**.

|  |  |
| --- | --- |
| (a) | Assume **VX = VY = 1.8 V**. Find value of **Vo** in volt. Find **IDX, IDY, IDL** and Power Dissipation. Verify the operating mode of **ML**. |
| (b) | Now, assume **VX = VY = 0.1 V**. Find value of **Vo**, **IDX, IDY, IDL.** |
| (c) | What should be the operating mode of **MX** and **MY** if **VX = 1.8V and VY = 0 V**? (Use logical reasoning, no need for calculation) |



## Question 3:

**The enhancement-load NMOS NOR gate in the figure is biased at VDD = 5.5 V. The transistor parameters are Kn = 0.2mA/V2 , VTN1 = 0.4 V, VTN2 = 1 V, VTN L = 0.9 V.**



|  |  |
| --- | --- |
| (a) | Find the operating mode of the load NMOS transistor. |
| (b) | Find the value of ***v*o in V and IDL, ID1, ID2 in *mA*** for ***vI*= 5.5V, *v2*= 5.5V** |
| (c) | Find the operating mode of the transistor **MD1.** |

## Question 4:

|  |  |
| --- | --- |
| (a) | A capacitor, C=100fF is charged from 0V to VDD Through resistor RP, where The PMOS W/L= 20; Find RP and the fall time tf for this circuit. |
| (b) | A capacitor, C=100fF is discharged from VDD to 0V Through resistor RN, where The NMOS W/L= 20; Find RN and the rise time tr for this circuit. |

## Question 5:

|  |  |
| --- | --- |
| (a) | Design a static CMOS logic circuit that implements the logic function ***Y= (AB+C)D*** |
| (b) | Design a static CMOS logic circuit that implements the logic function ***Y= (A+B)CD*** |
| (c) | Design a static CMOS logic circuit that implements the logic function ***Y= F(AB+C(D+E))*** |

## Question 6:

Design a CMOS logic circuit to implement the given compound gate in Figure below. First derive the logical expression of output Y and then design the CMOS network.

